KEYSIGHT WORLD 2019

Evolution of High-Speed Server and Computing Interfaces

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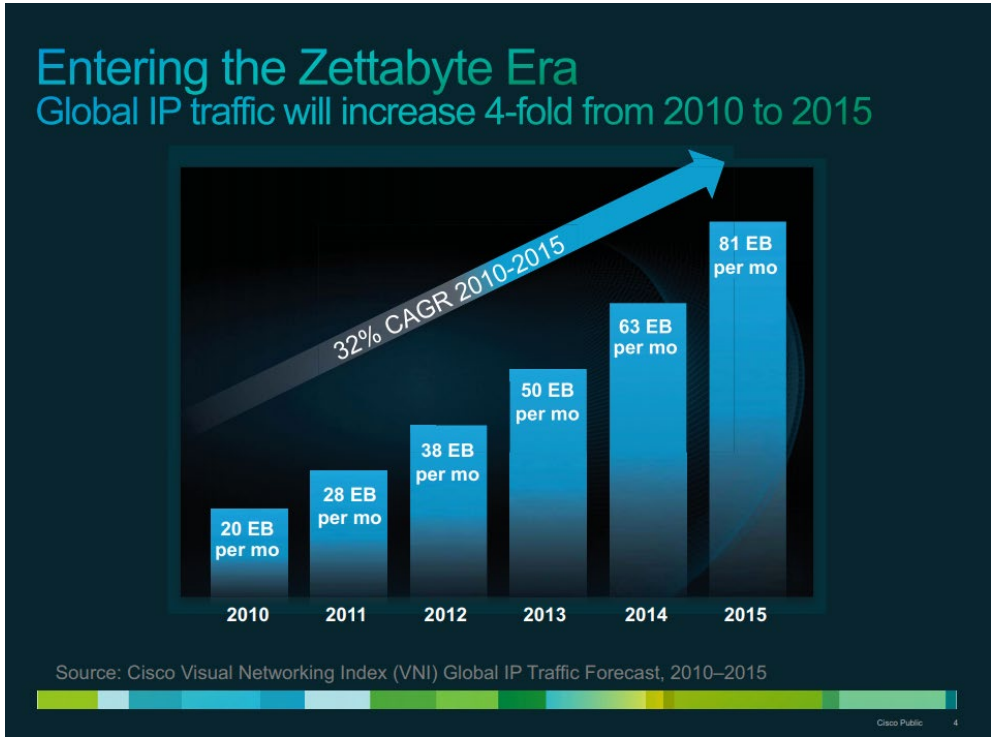
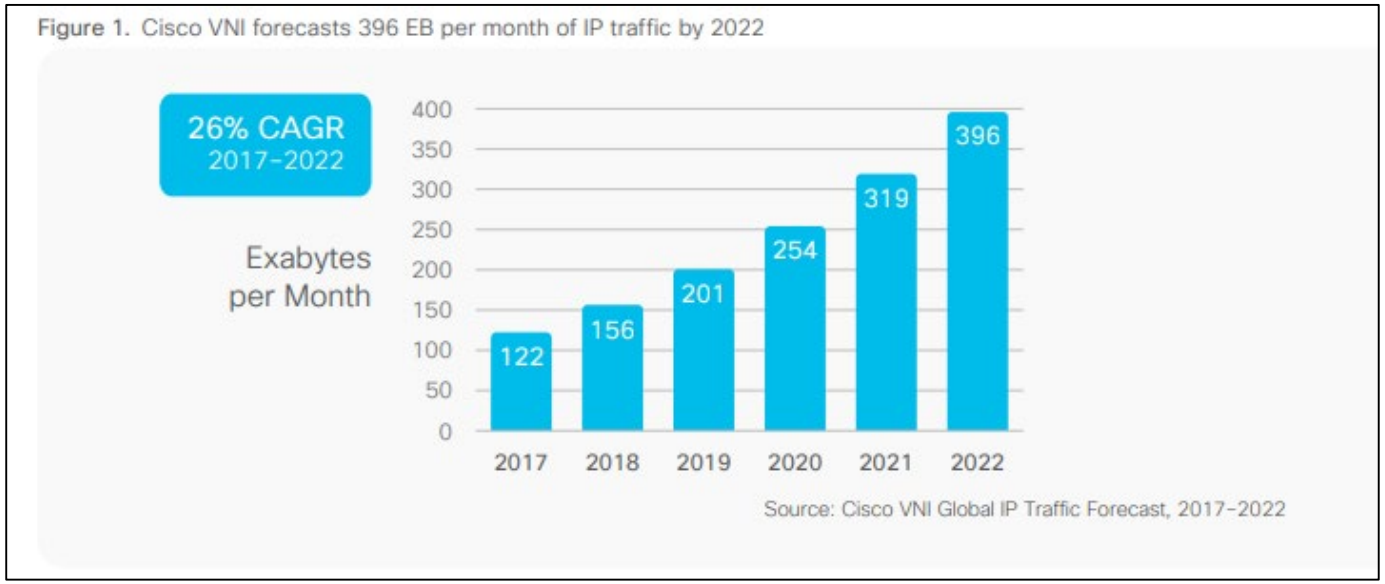
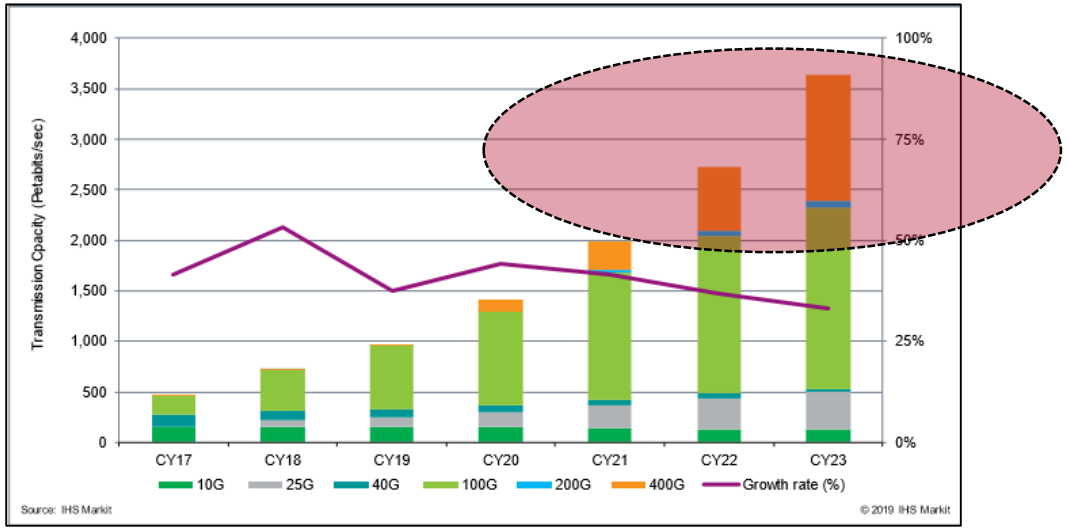
Senior Application Consultant/ Keysight Technologies

The New Age… Digital is Being Pushed

PREDICTIONS ARE HOLDING TRUE- INVESTMENTS ARE REQUIRED



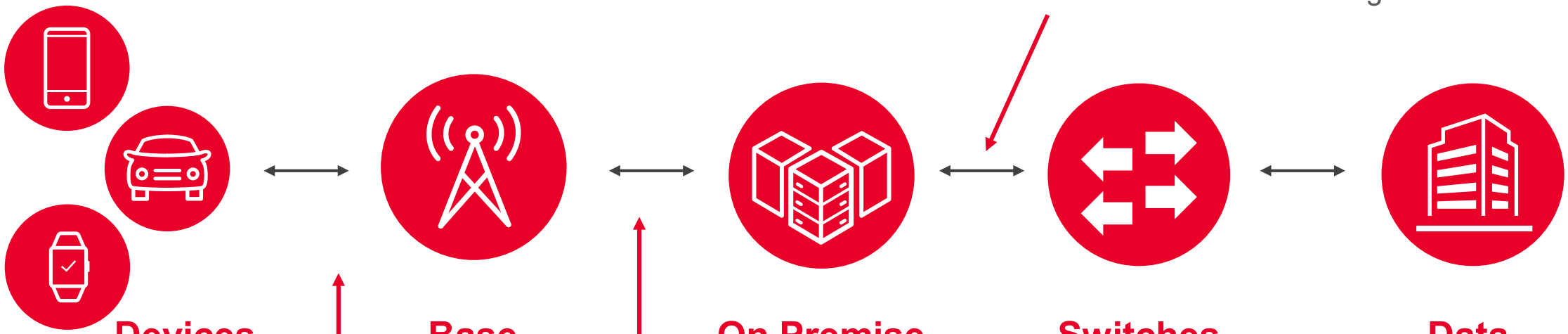




- 400GbE is happening, IP traffic predictions continue to show strong growth worldwide.
- Now is an opportunity to grow and take market share.

An Overhaul of the Entire Infrastructure

- Network capacity crunch drives the need to push more data through the same channel
- New data schemes emerge



Devices

- 5G acceleration: China/6GHz leading, mmWave following
- Small cell and Wi-Fi integration drive the complexity of network test

Base Station

- Mobile Edge Computing grows rapidly - data center traffic moves to the base-band unit (BBU)
- Drives the need for fronthaul analysis, eCPRI takes over

On Premise Server

Switches

- Increased data loads drive the need for faster switching speeds - 400G gives way to 800G

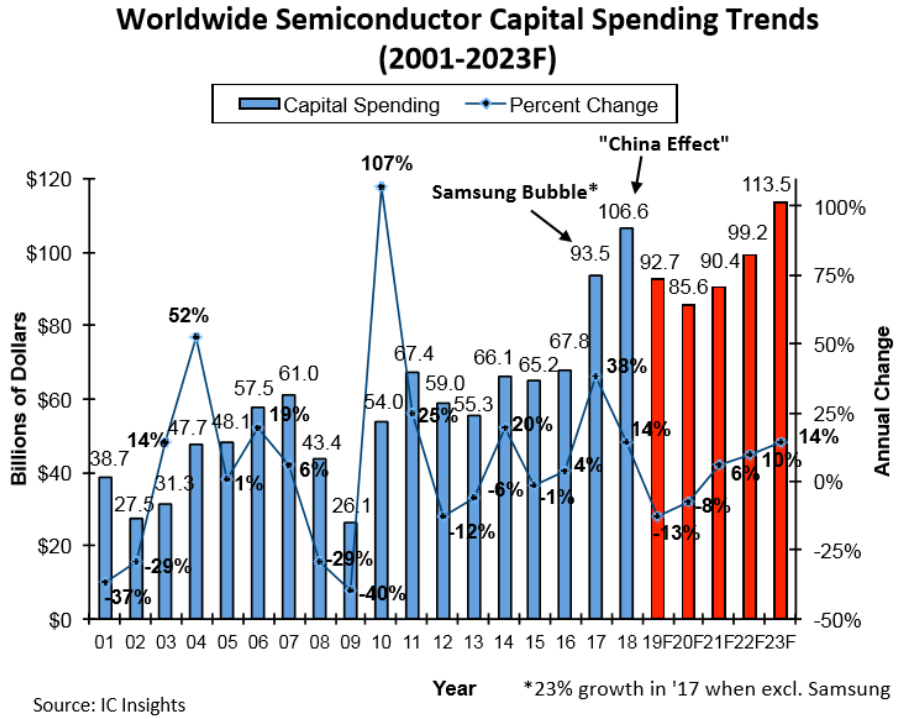
Data Center

- Hyperscaling increases speeds throughout the data center
- New switch architectures are defined
- New standards emerge (CCIX, GenZ, OpenCAPI, gen5)

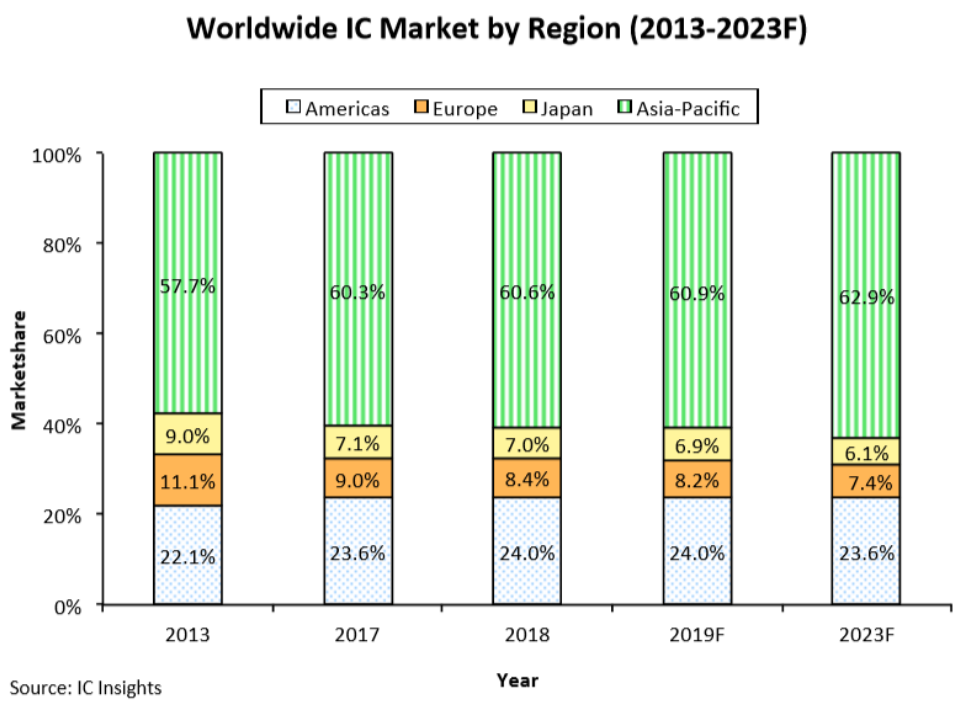
The Perfect Opportunity to Gain Market Share

DISRUPTIONS ABOUND – INVEST AND WIN

- CAPEX spending is increasing worldwide
- To keep pace, you must purchase equipment that will enable you to be successful
- The right equipment will give you a strong competitive advantage, but you must be willing to spend



Source: IC Insights



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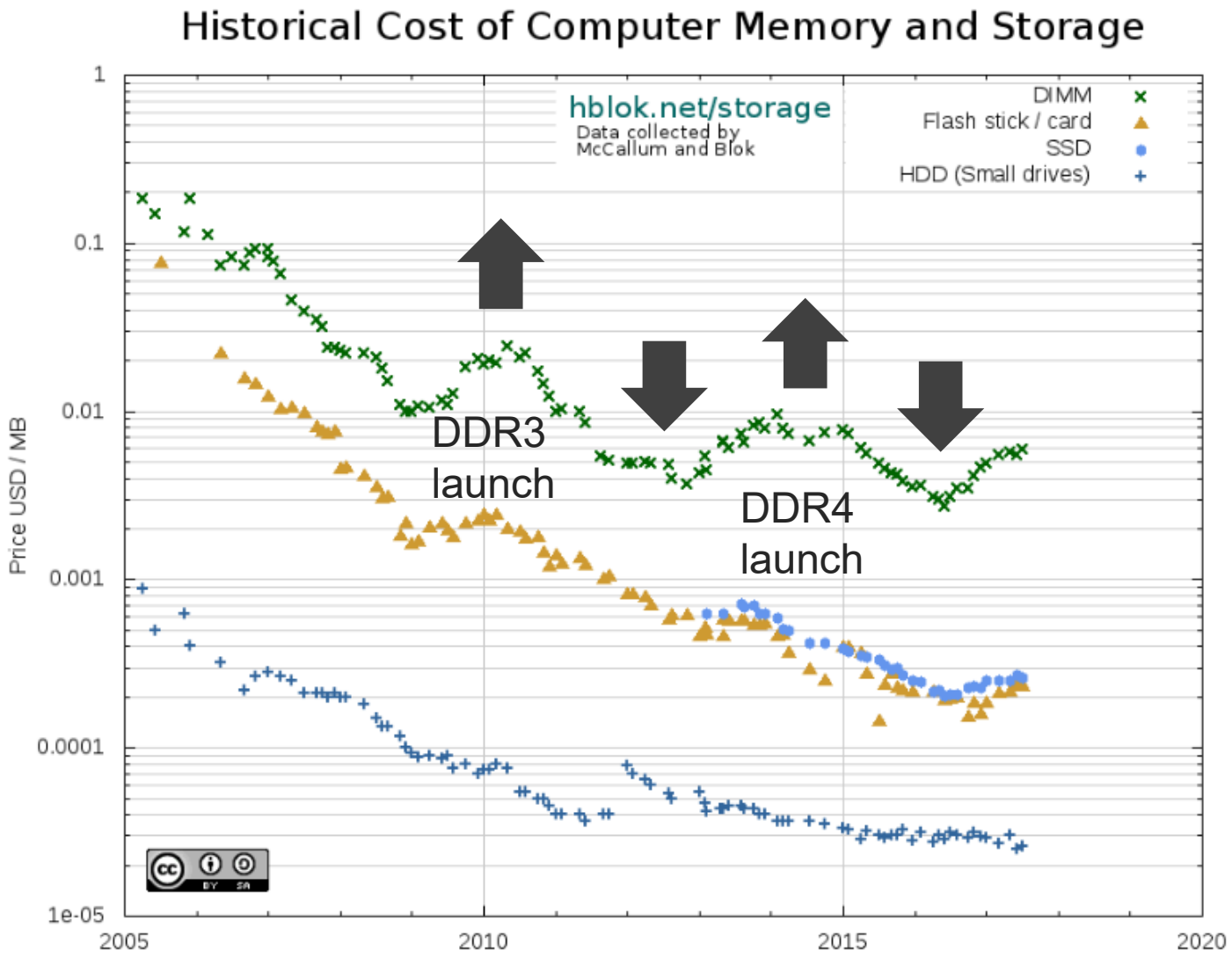
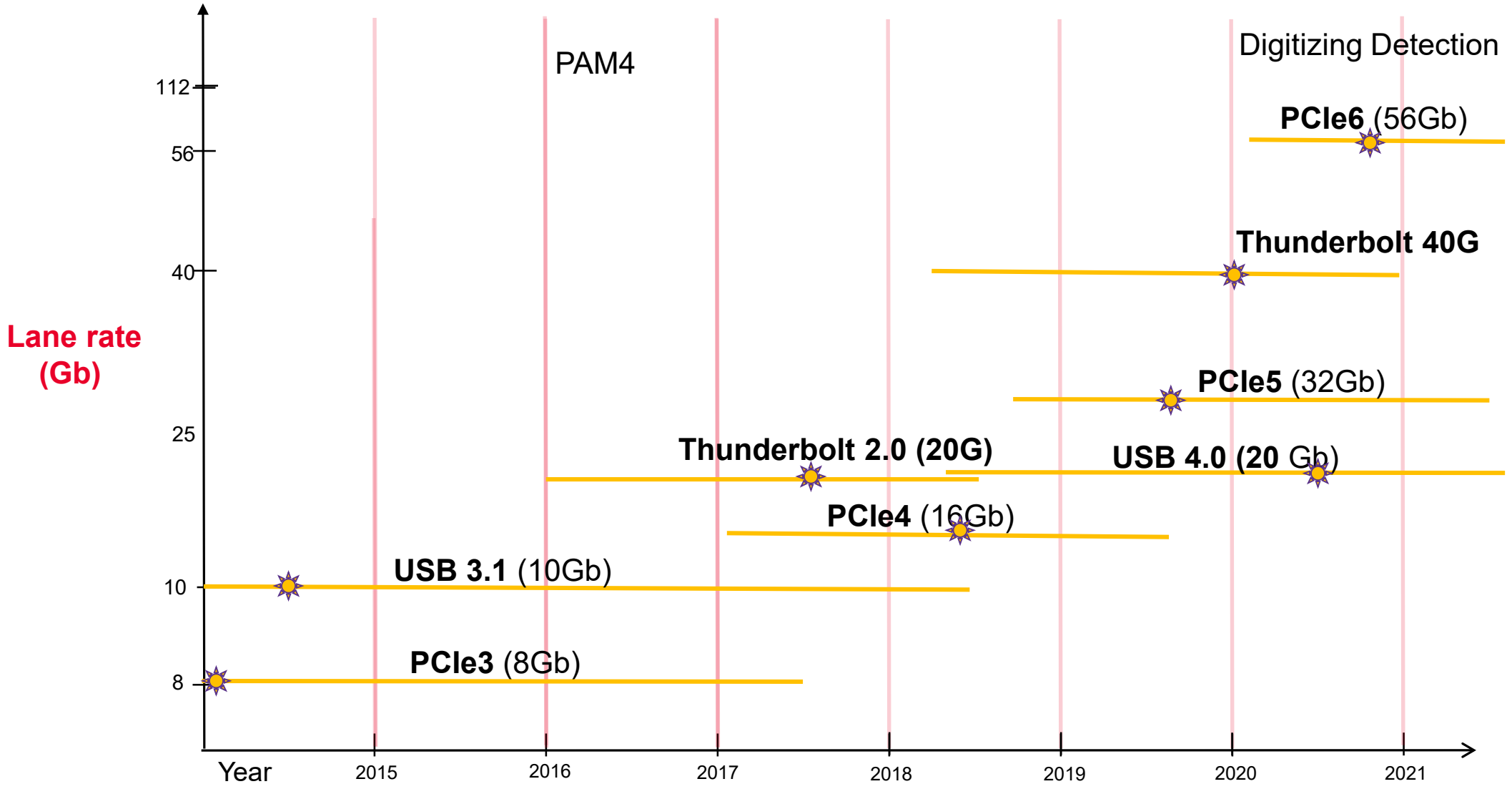
First to Market Advantage



High speed digital roadmap requiring UXR purchase

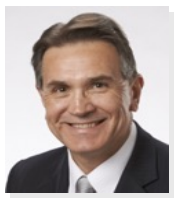


Keysight Participation in Standards

TRUST OUR EXPERTISE

Memory Perry Keller	DisplayPort Brian Fetz	USB Jit Lim	Computer Rick Eads	Optical Comp. Greg LeCheminant	Optical WAN Stefan Loeffler	HDMI Brian Fetz	400G Steve Sekel	MIPI Roland Scherzinger
Board of Directors JEDEC Compliance Chair	Contributor Board Alumni, VESA Phy Sub Group Compliance	Contributor USB-IF Thunderbolt	Board of Directors PCI-SIG Contributor CCIX GenZ	Contributor IEEE, OIF- CEI, T11 FC	Contributor OIF, ITU, IEC	Contributor HDMI	Contributor IEEE, OIF, 64G FC	TSG Member UniPro Vice Chair MIPI Alliance Thunderbolt
DDR UFS	DP 1.3 Type C	USB 2.0, 3.0, 3.1	PCIe G3, G4, PAM4 (RT)	PAM4 (Opt), CEI 3.1	PAM4 (Opt), CEI 3.1	HDMI 2.0	IEEE802.3bs, IEEE802.3by	D/M/C–PHY, UniPro,TBT






Changes in High-Speed Digital Buses

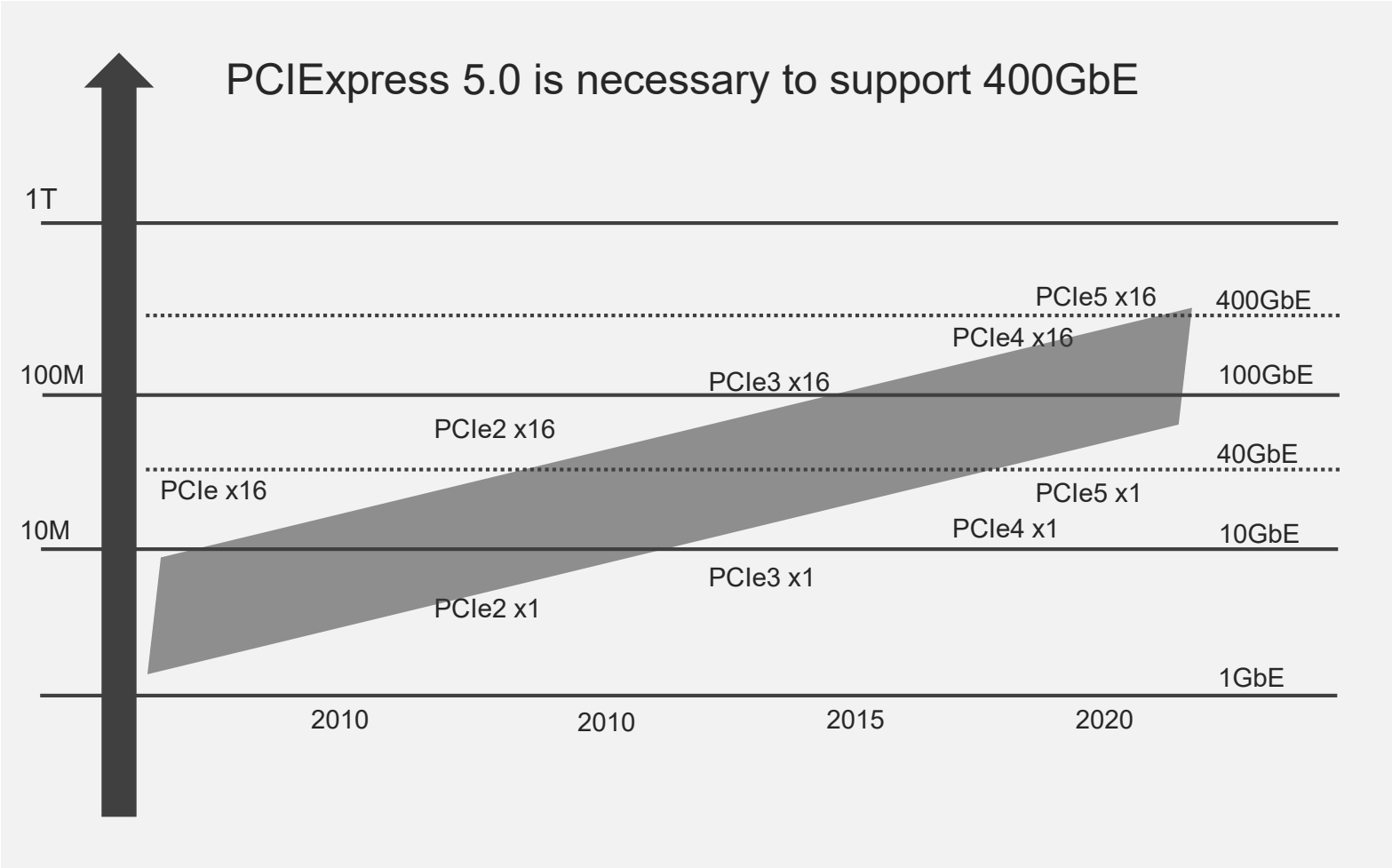
DISRUPTIONS OFFER OPPORTUNITIES

- DDR / LPDDR are moving to DDR / LPDDR5
- PCI Express (PCIe) is moving to PCIe Gen5
- Emergence of new computing standards (CCIX, GenZ, CXL, OpenCAPI)

PCI Express Gen5 – Moving to 32 Gbps

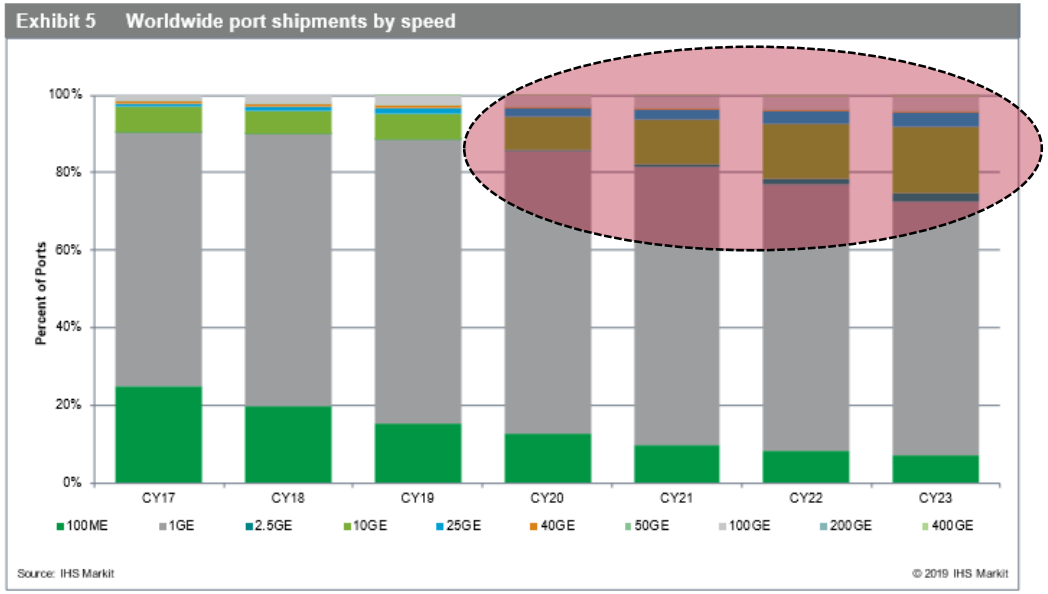
Drivers of PCIe 5.0 Performance

- High-end networking
  - 400 Gb Ethernet
  - Dual 200 Gb/s InfiniBand
- Storage Networking
  - NVM Express (NVMe)
  - Big Data
- Increased IC I/O Speeds
  - Co-Processors (FPGA, GPU)
  - ASIC
  - IP
  - Artificial Intelligence Engines



Industry Drives Higher PCIe Bandwidth Requirements

- PCIe 5.0 = 32 Gb/s
- Required for 400 Gb Ethernet
  - This equates to 50 GB bidirectionally
  - 16 lanes gives up to 64 GB/s
  - Total full duplex BW = 128 GB/s
- CEM connector for PCIe 5 is planned to be backward compatible with earlier PCIe technologies.
- Spec releases at the end of 2019



Early 400G investment taking place

	Raw Bit Rate/Lane	Link BW	BW/Lane	Total x16 Bi-Directional Bandwidth
PCIe 1.x	2.5 GT/s	2 Gb/s	250 MB/s	8 GB/s
PCIe 2.x	5.0 GT/s	4 Gb/s	500 MB/s	16 GB/s
PCIe 3.x	8.0 GT/s	8 Gb/s	~1 GB/s	~32 GB/s
PCIe 4.x	16.0 GT/s	16 Gb/s	~2 GB/s	~64 GB/s
PCIe 5.x	32.0 GT/s	32 Gb/s	~4 GB/s	~128 GB/s

PCI Express Technology Roadmap

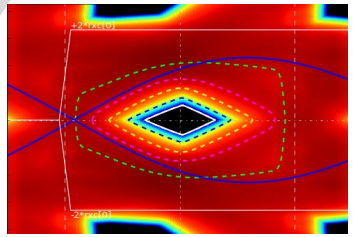
2019
PCIe 5.0 (32 GT/s)

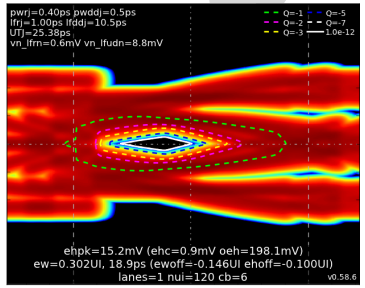
2017
PCIe 4.0 (16 GT/s)

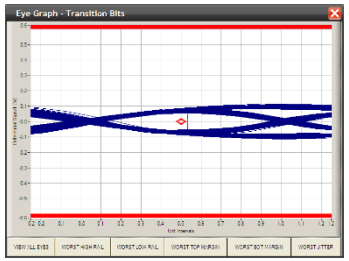
2010
PCIe 3.0 (8 GT/s)

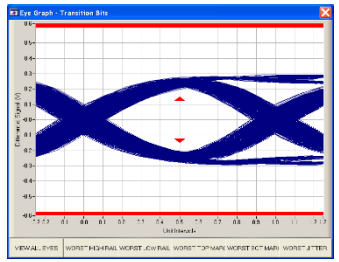
2006
PCIe 2.0 (5 GT/s)

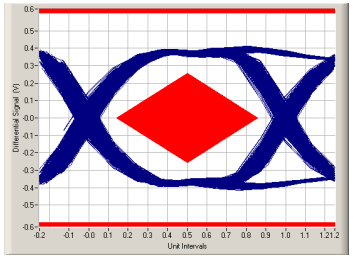
2003
PCIe 1.0 (2.5 GT/s)

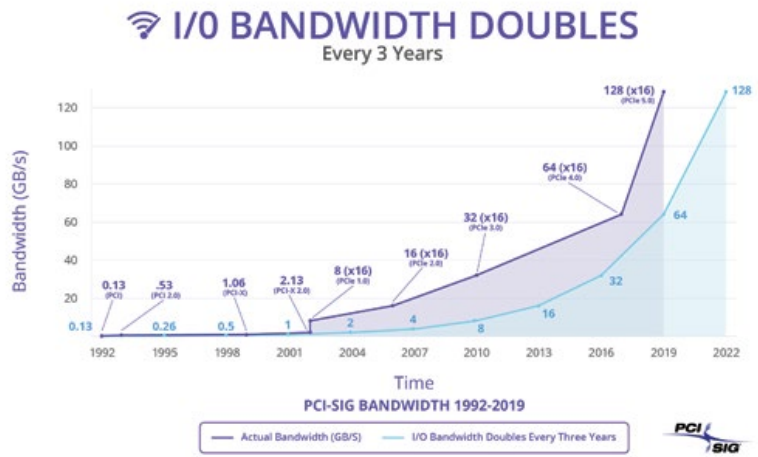












Breakthrough Technology

ENABLES 1-TERABIT/S MEASUREMENTS

Introducing UXR-Series Ultra-High Performance Infiniium Oscilloscopes

110 GHz maximum bandwidth with
extremely high signal integrity

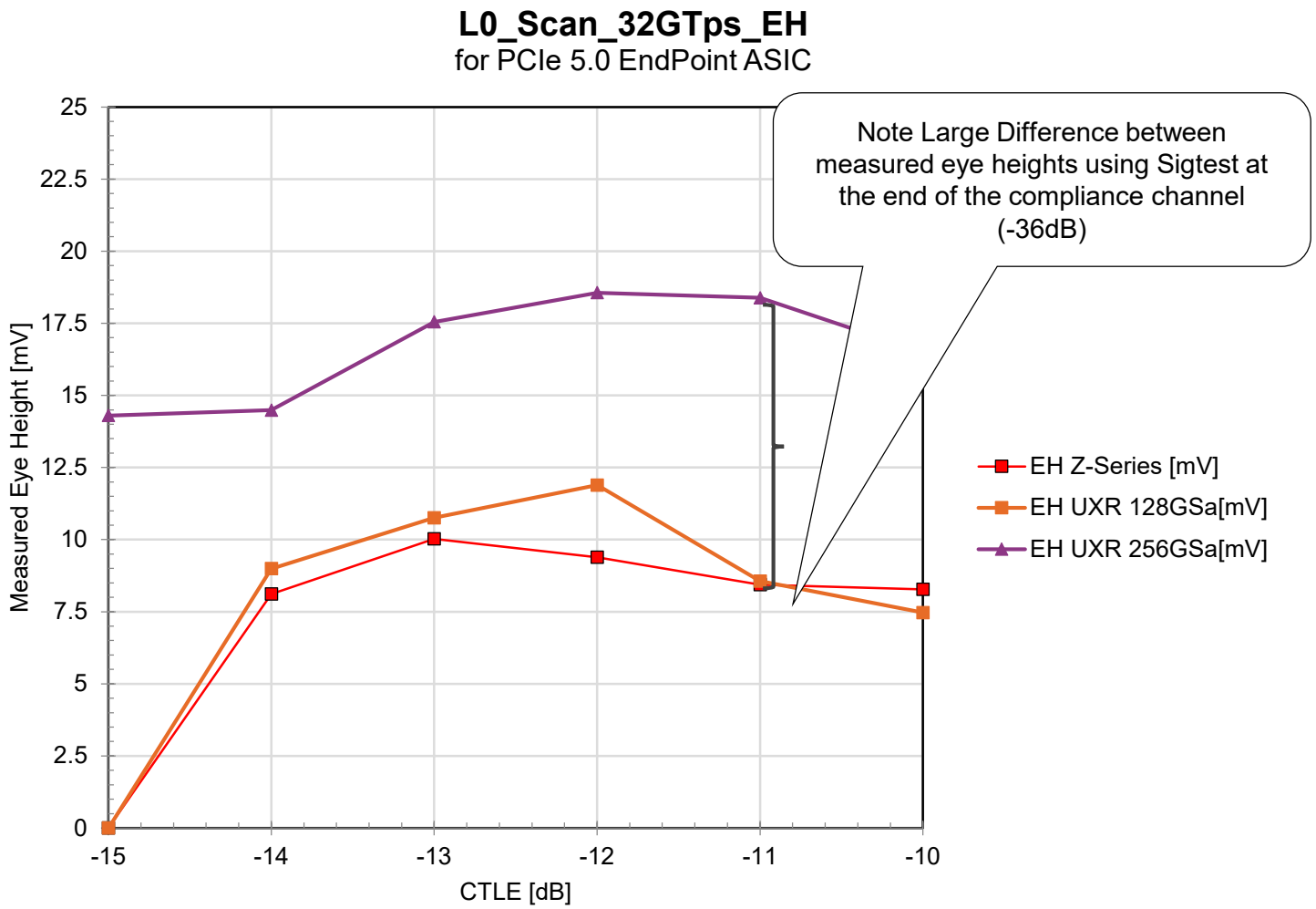
- 13 – 110 GHz models
  (on all channels)
- 256 GSa/s on all channels
- 2G max memory per channel
- 10-bit ADC and superior ENOB with extremely low noise
- Vertical sensitivity from 10 mV to 500 mV per division
- 2 or 4 channels
- Full self-calibration

A Real Life Story

REDESIGNS IMPACT SCHEDULE

- During development of the UXR oscilloscope, Keysight had to make multiple design changes to remove clock coupling in its channel path
- The redesigns cost valuable time to market in a hot economy.

UXR vs Z Series: End of Channel Results



- Data Rate = 32 Gb/s
- Sigtest Composite Eye Height
  - 2M UI
  - CTLE -10dB to -15dB
- M8040A BERT
  - TX preset P5
  - Generator Launch =800mV
  - DMSI=10mV
  - CMSI=0mV
  - RJ=0.5ps
  - SJ=3.125ps @ 100MHz

The need to invest correctly to win in PCIe 5.0

MASTER YOUR BEST DESIGN

- Bandwidth Bandwidth Bandwidth
- Extremely small eyes, instrument noise matters
- Receiver calibration
- Gen6 is right around the corner to enable 800G

D9050PCIC New Features

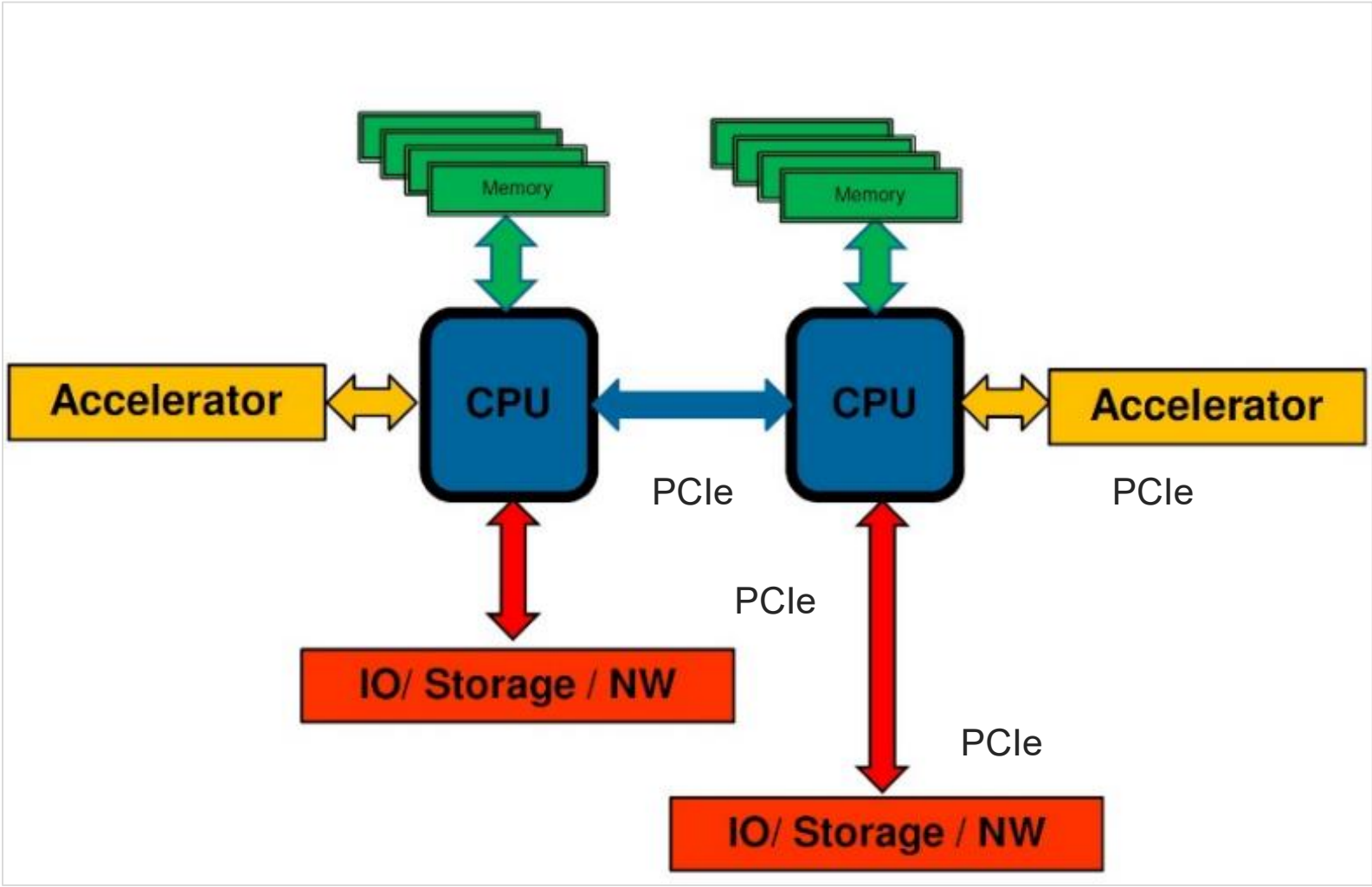
MASTER YOUR BEST DESIGN

- Supports PCIe 5.0 BASE TX Testing at 32 GT/s as well as 2.5G, 5G, 8G and 16 GT/s (v0.9 BASE)
- Supports PCIe 5.0 Reference Clock tests (2.5G, 5G, 8G, 16G)
- Will Support CEM tests for endpoints and root complexes (2.5G, 5G, 8G, 16G, 32G).
- Integrated De-embedding of break-out channel with optional InfiniiSim
- Automated DUT control using an 81150/60A Pulse Generator ARB.
- Enhanced Switch Matrix supporting arbitrary lane mapping
- Minimum oscilloscope BW: 50 GHz

The Emergence of New Technologies - Beyond 32 Gbps

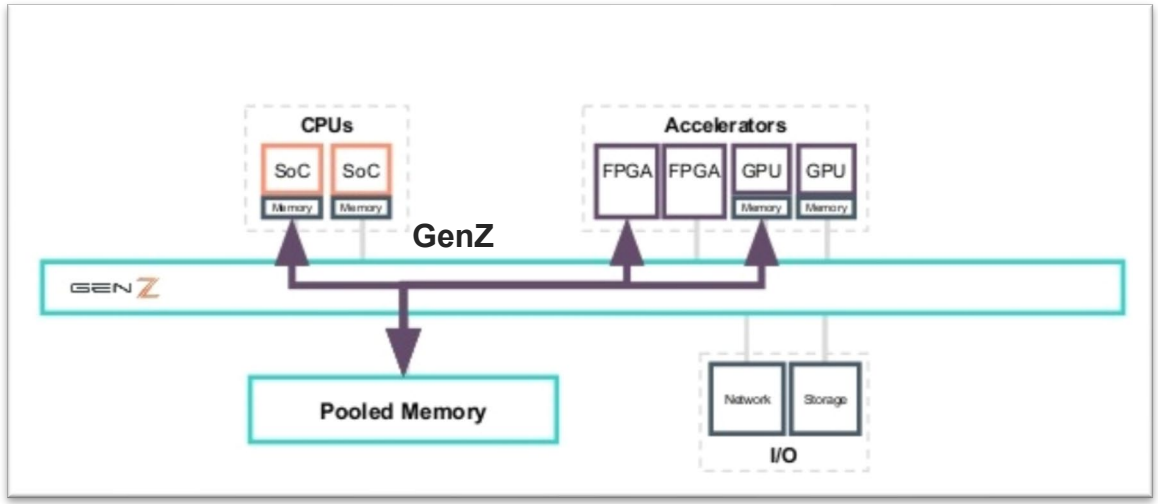
Next-Generation Computer Architecture Examples

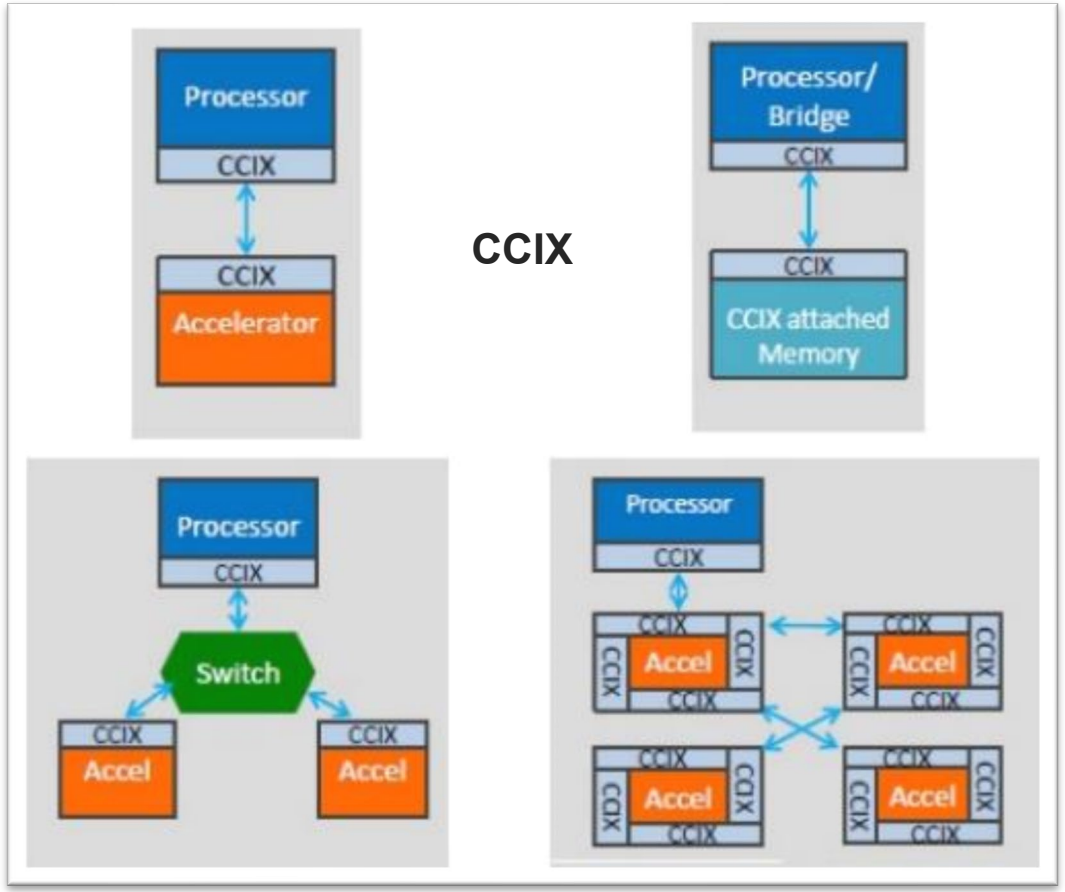
Typical Two CPU Architecture 2017



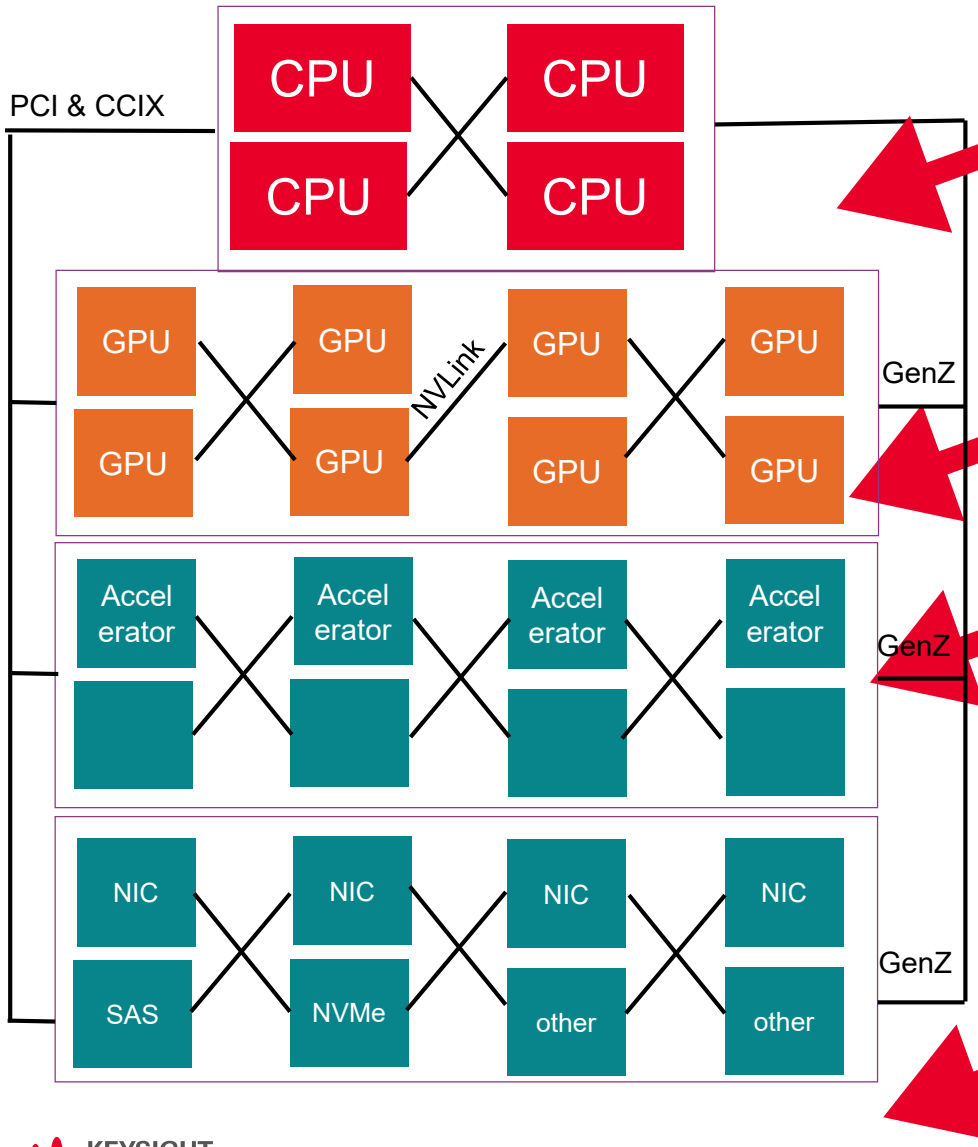
Next-Generation Computer Architecture Examples

Computer Architecture 2018-2021





Server Advancements come 2019



PCI Express / CCIX offer a choice to designers for CPU to accelerator communication

NVLINK replaces PCI Express for GPU to GPU communication running at >25 Gbps

PCI Express / GenZ battle for communications between memory and CPU

DDR4 is replaced by DDR5 for memory. LPDDR4 gives way to LPDDR5

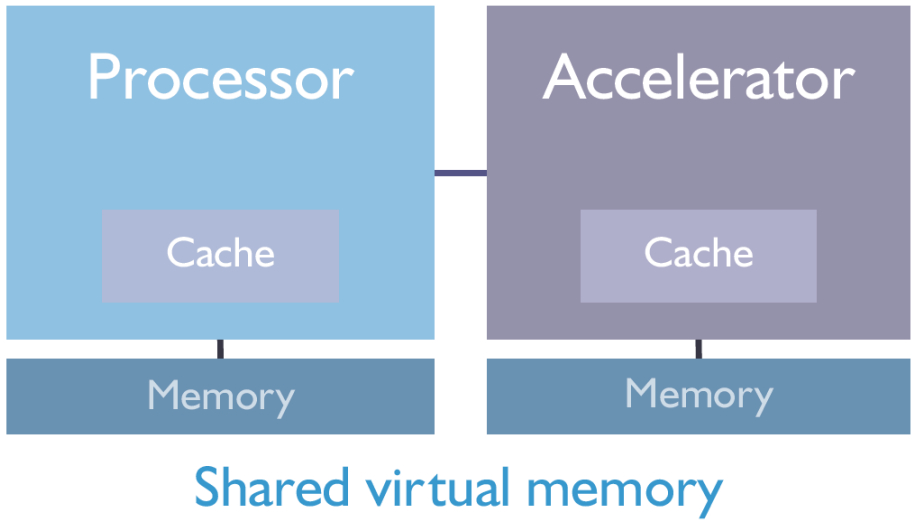
OPENCAPI and other technologies push for the fabric of the server

Intel announces new CXL open bus for coherency

Cache Coherent Interconnect for Accelerators

CCIX

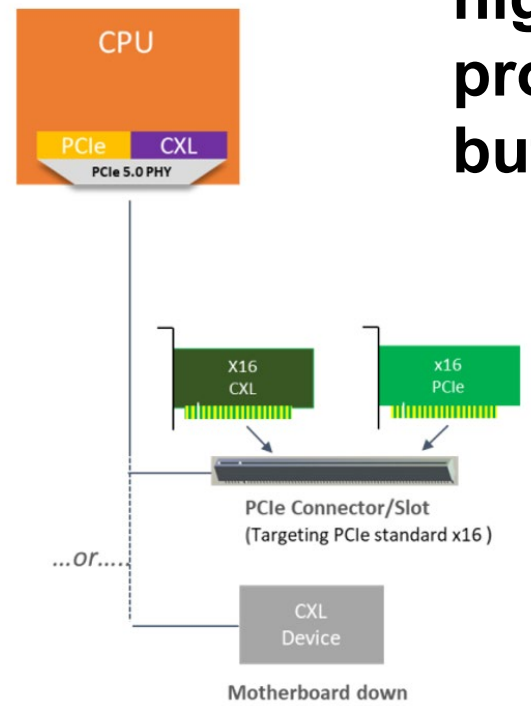
CCIX™ is a chip-to-chip interconnect that enables two or more devices to share data in a cache coherent manner



- Machine Learning and Big Data applications are fundamentally changing the way that the processing of data happens
- Industry questioning whether CCIX will be able to access CPU cache data (proprietary to CPU vendor?)
- CCIX will leverage PCIe Gen5 for their next speed bump above 25 GT/s
- CCIX is pathfinding the use of PAM4 for computer I/O interconnect use.

Compute Express Link

CXL



Compute Express Link has the benefit of supporting both standard PCIe devices as well as CXL devices – all on the same Link

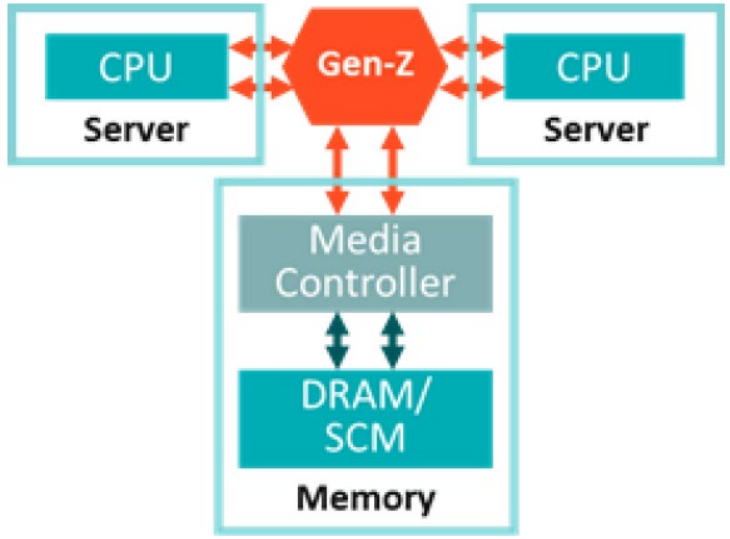
CXL is an open industry standard interconnect offering high-bandwidth, low latency connectivity between host processor and devices such as accelerators, memory buffers, and smart I/O device

- Developed as an open community to allow access of the CPU cache
- Bus is similar to a bus known as QPI, the difference is that this is open where QPI was closed
- By leveraging the PCIExpress Phy, adoption to CXL is fairly easy as no new Phy testing is required

Gen-Z

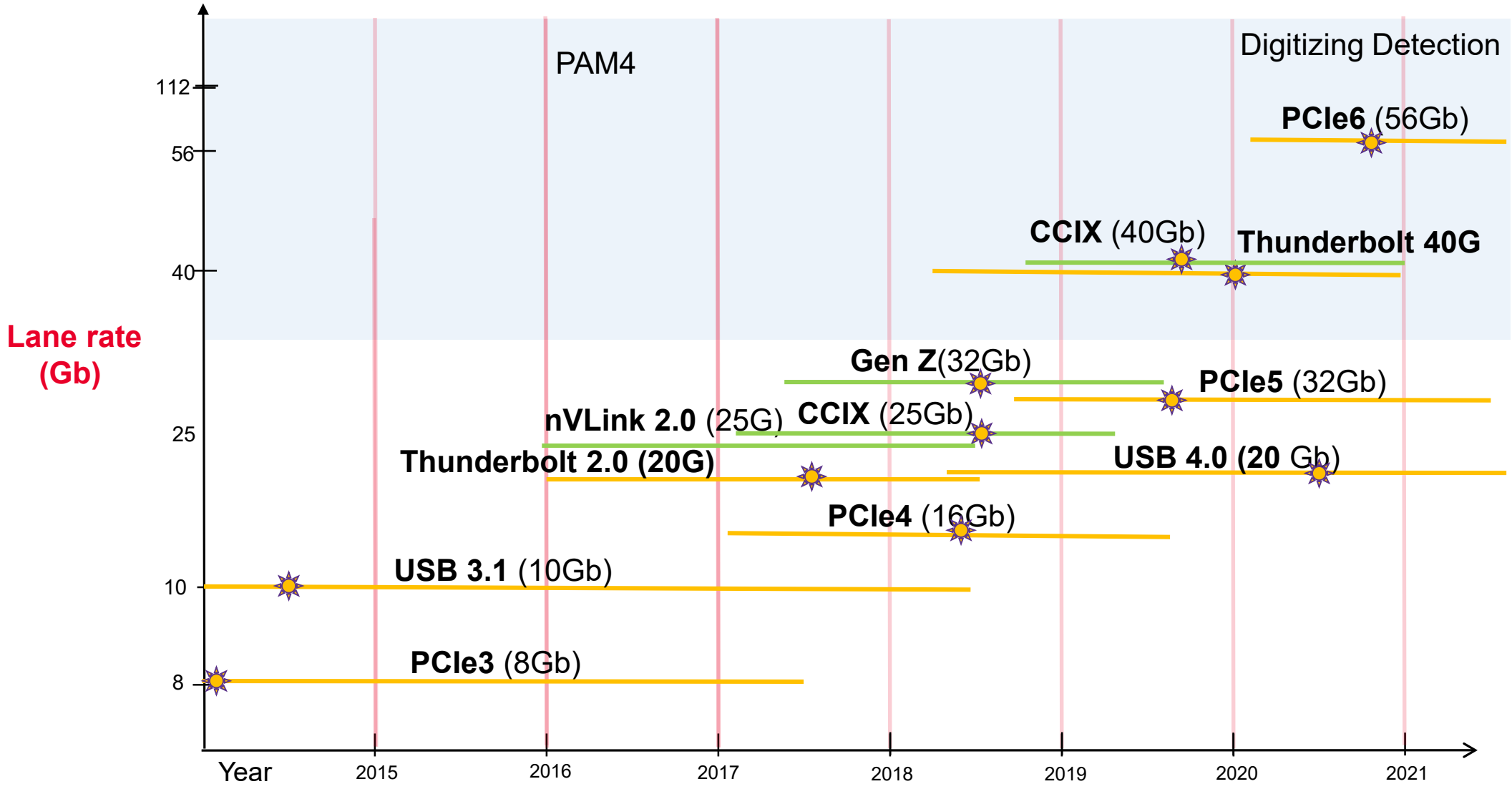
WHAT IS IT?

Gen-Z is a data access technology that provides a framework for both optimized and traditional data storage messaging solutions



- Gen-Z is attempting to revolutionize computer architecture
- It is a memory centric architecture leveraging 90% of compute happens off-CPU
- Keysight is co-chair of Gen-Z CIWG

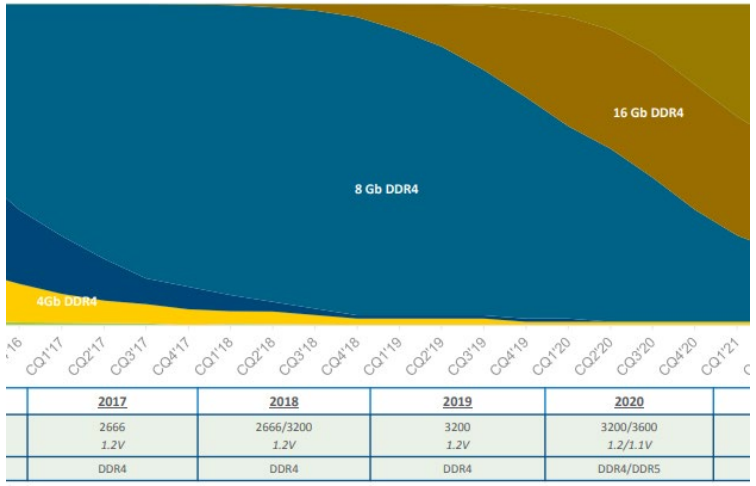
High-Speed Computing Roadmap



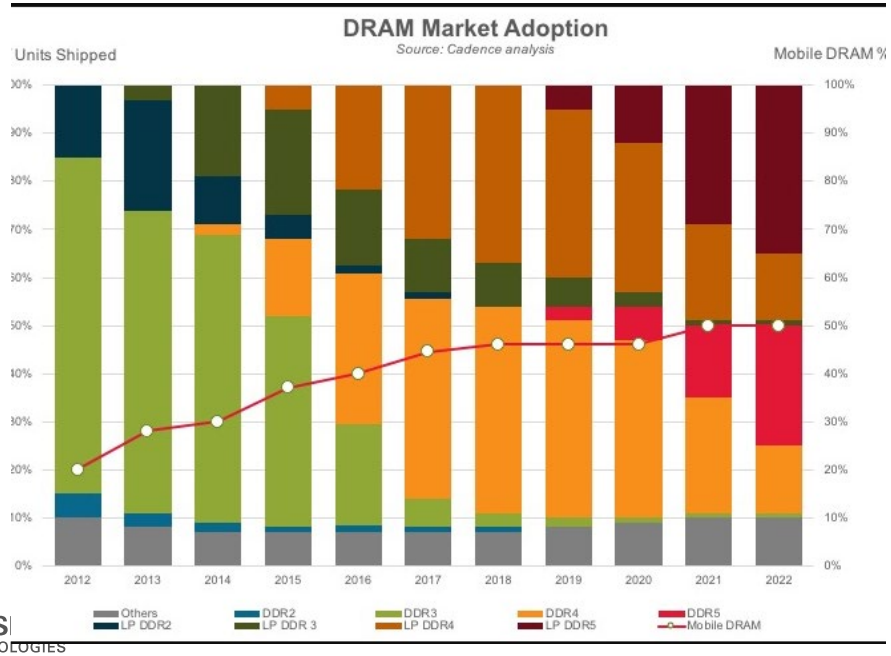
DDR5 – Bring on Rx Testing

Differentiation Drives Higher Profits

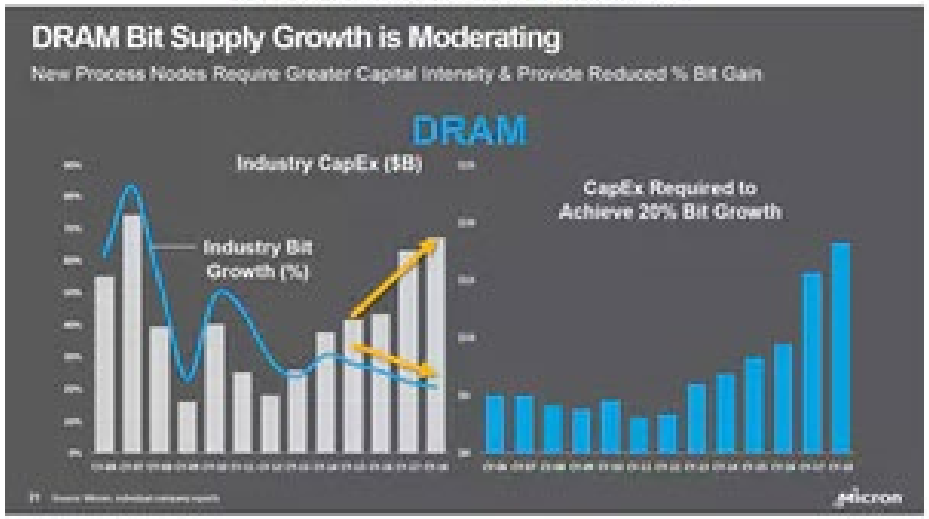
FIRST TO MARKET DDR5



2017	2018	2019	2020
2666 *1.2V*	2666/3200 *1.2V*	3200 *1.2V*	3200/3600 *1.2/1.1V*
DDR4	DDR4	DDR4	DDR4/DDR5



Micron's Forecast for DRAM Industry Supply



The New Age - DDR Signaling Evolution

DDR6?

"Light Speed"
- Complex modulation?

IQ Threshold

DDR5

"Hyper Speed" - No visible eye
- Pre/De-Emphasis, Impulse response

Impulse Response Threshold

DDR4

"Serial Speed" - Clock often embedded
- Eye Diagrams/Masks
- Error rates, Jitter/Noise

Jitter & Noise Threshold

DDR3

DDR2

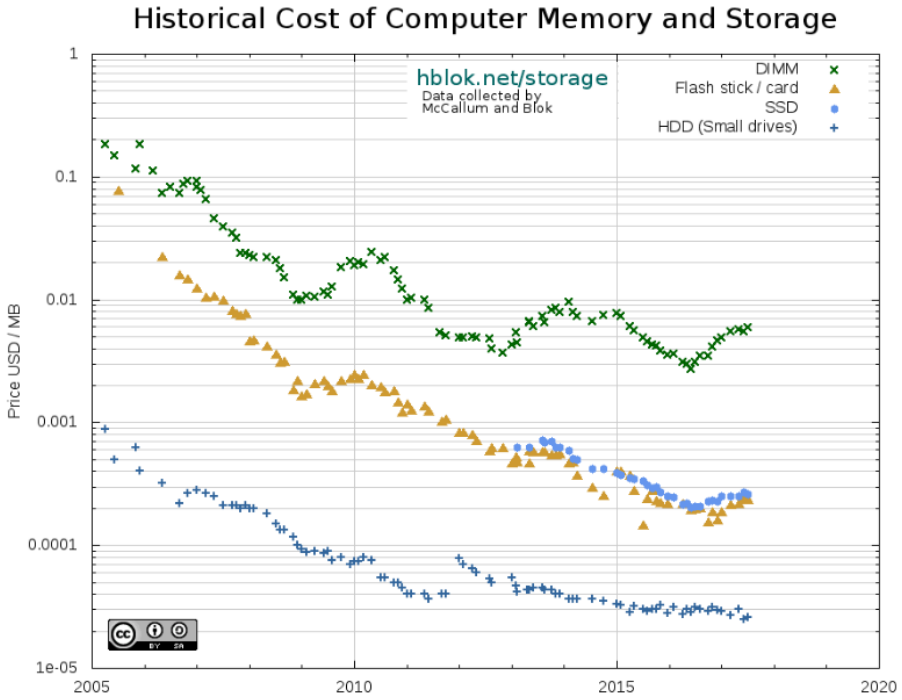
DDR

"High Speed" - Transmission lines
- Timing
- Impedance / load curves

Signal Integrity Threshold

Static RAM

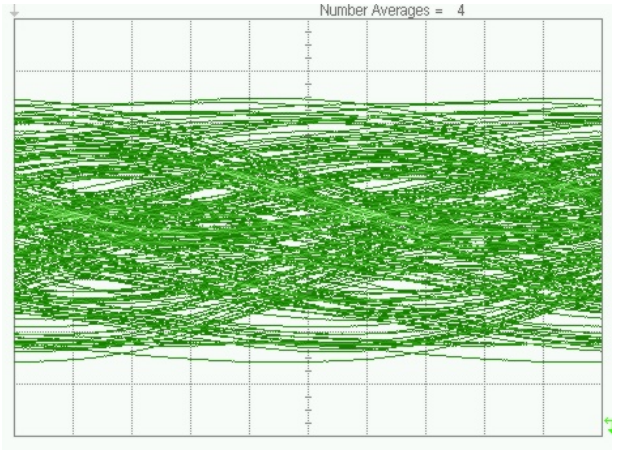
"Low Speed" - Auto place and route
- Fanout
- Capacitance



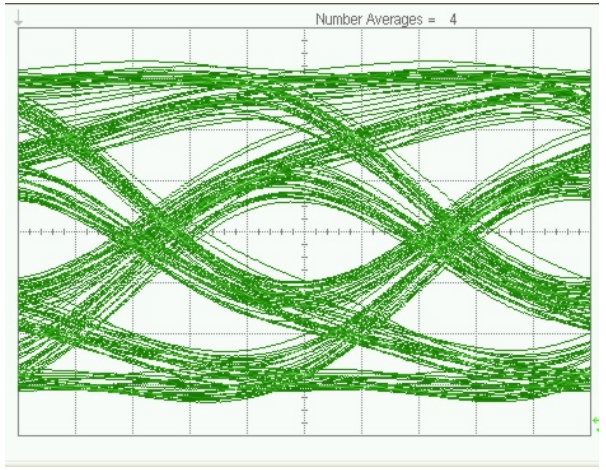
New to DDR5

EQUALIZATION

Closed eye



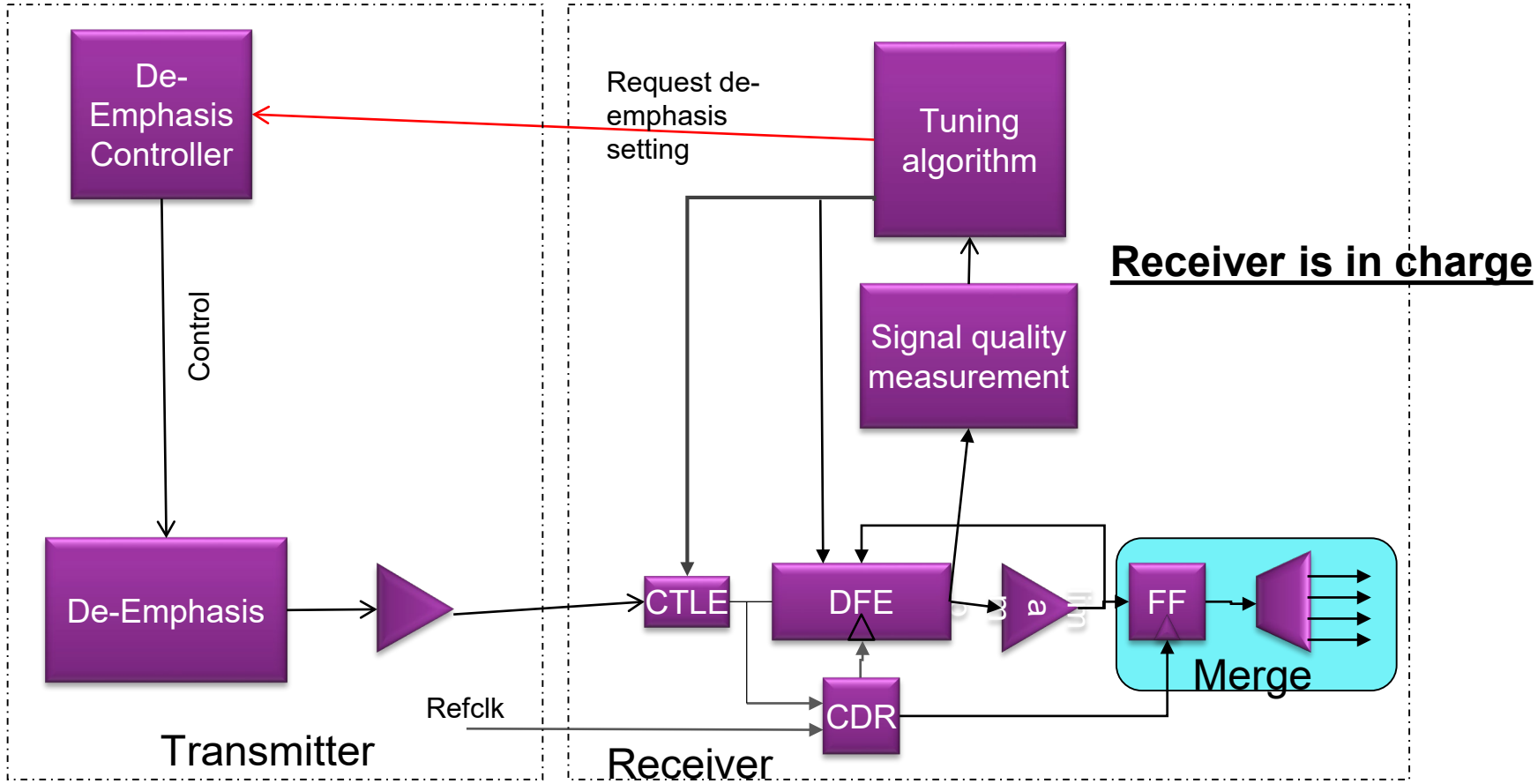
Open eye



A whole new game for memory

Receiver Testing Begins in DRAM

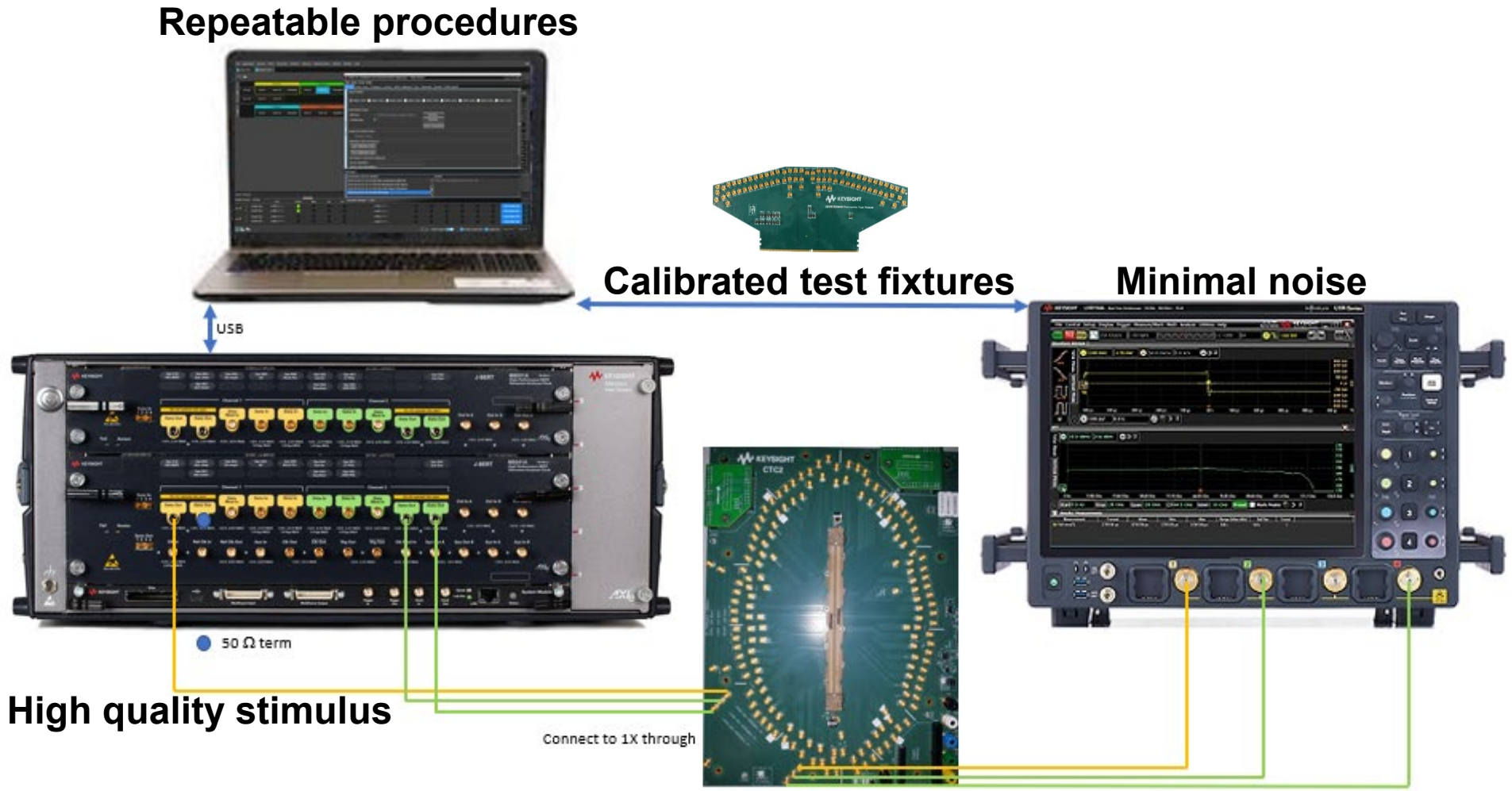
SMART RX EQUALIZATION (PCI-E)



Rx is a “Black Box” and must accept any compliant signal

Keeping up with the market

INVESTMENT IN RX EQUIPMENT MUST BE MADE



The Perfect Opportunity to Gain Market Share

DISRUPTIONS ABOUND – INVEST AND WIN

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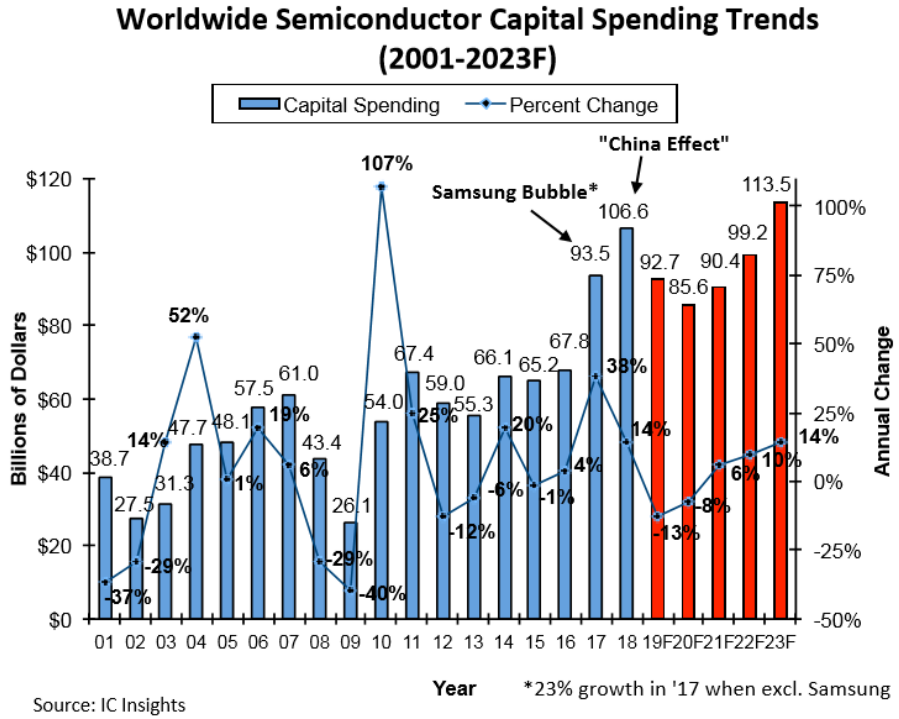
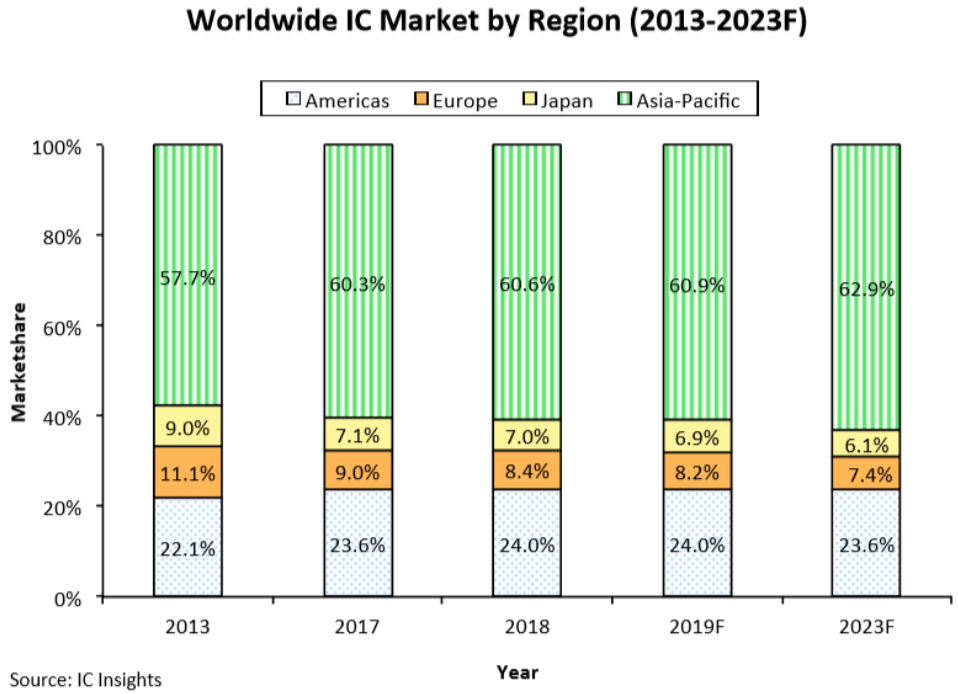
- To keep pace, you must purchase equipment that will enable you to be successful
- The right equipment will give you a strong competitive advantage, but you must be willing to spend





Additional Resources

- Learn more about Keysight's High-Speed Digital System Design solutions
- Download the following white papers:
  - Evolution of High-Speed Computing Interfaces: Paving the Way for 400GE in the Data Center
  - The Fast Track to PCIe 5.0: Doubling the Throughput of PCIe 4.0 to 32 GT/s
  - DDR5 - Full Speed Ahead to 400GE: Faster Networking Speeds Require Faster Memory
- Register for Data Center webinars from Keysight

USB 3.2/4.0 – Possible Convergence of Multiple Technologies

Industry Drivers for USB Type-C

- New form-factor
  - Smaller size
  - Reversible plug orientation
  - Reversible cable direction
- Establishes power delivery
  - Scalable charging to 100W
  - Power direction, data direction, Vconn swap
- Enables adoption by other standards
  - ALT (Thunderbolt, DisplayPort, MHL, HDMI) and Accessory Mode (Audio)
  - Future scalability
- Legacy Compatibility
  - USB 2.0, USB 3.1 Gen 1, BC 1.2
  - 5V Vbus start

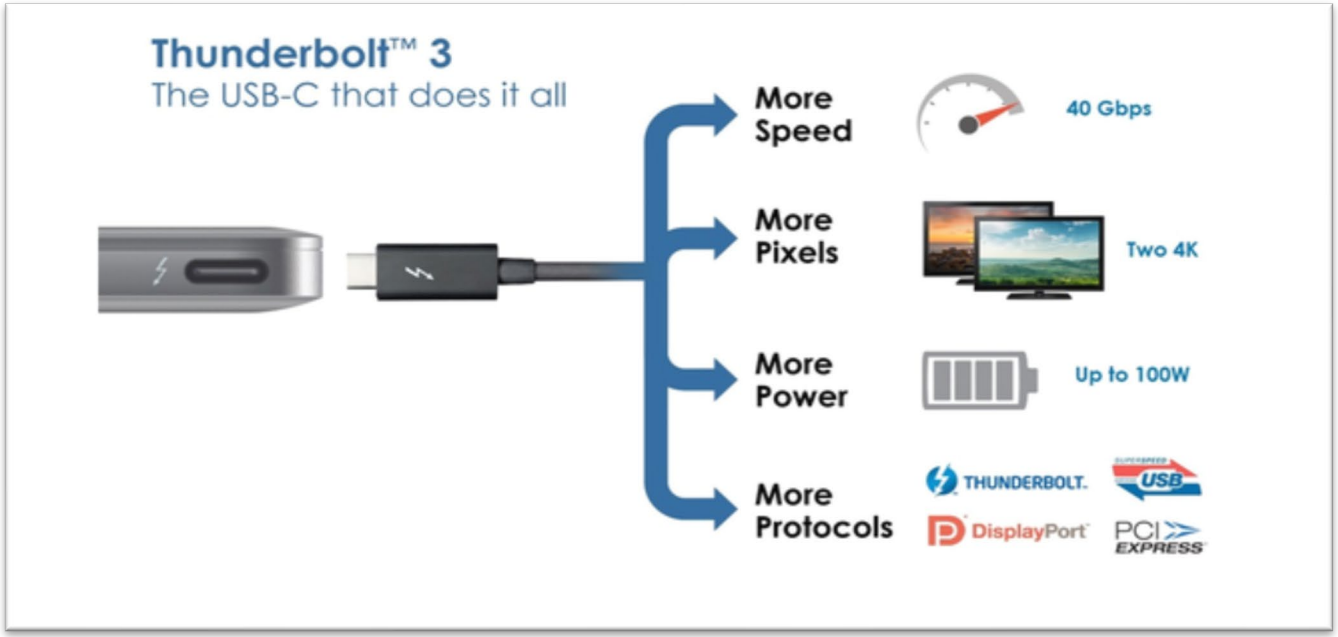
USB4 Overview

- Announced by USB-IF in Q1 2019
- Based on the Thunderbolt 3 protocol
- Uses the Type-C connector
- Tunnels USB, DP, and PCIe
- Channel aggregation: two independent 20Gbps bonded into one logical 40Gbps link
- Supports other standards through ALT mode
- Keysight can help test Protocol Decode, TX, RX, and Return Loss
- Open standard and integrated in CPU

Universal Serial Bus 4 (USB4)
Specification

USB 4.0 Merges into Thunderbolt 3.0

- Announced in 2018
- Uses the Type-C connector
- Channel aggregation: two independent 20 Gb/s links into one logical 40 Gb/s link
- Supports other standards through ALT mode
- Cost competitive vs multi-chip, discrete, mux solutions
- Keysight can help test TX, RX, and Return Loss
- Open standard and integrated in CPU



USB4 Electrical Testing Methodology

- PHY testing approach will be similar to Thunderbolt 3
  - Tx, Rx, and Return Loss
  - Active and Passive Cable Test

  Plus
  - Type-C Power Delivery
  - DP, USB over Type-C

Universal Serial Bus 4 (USB Type-C)
Electrical Compliance Test Specification

Proposed differences between testing USB 3.2 x1 vs USB4

- Return Loss TX and RX
- Transmitter Equalization is not fixed and requires calibration
- Receiver Equalization is much more complex and requires calibration
- PHY bit rate doubles from 10 Gbps to 20 Gbps
- Signaling on all 4 Type-C high-speed pairs
- De-Embedding of Test Cables
- Retimer specific measurements
- Cross-talk Generation
- New Jitter Measurements
- New Phase and Slew Rate Measurements
- Added Skew Measurements
- Common Mode and Differential Mode Interference
- Separate Jitter Cocktails for 10G/20G/TP1/TP3EQ
- Link Optimization prior to BER test
- Built in Error Detector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